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PATENT  
Attorney Docket No. 011775-013210US

TOWNSEND and TOWNSEND and CREW LLP

By: /Kelly Pedersen/

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Subhas C. Bose Jayappa Veeramma et al.

Application No.: 10/650,451

Filed: August 27, 2003

For: IMPROVING BREAKDOWN  
VOLTAGE FOR POWER DEVICES

Confirmation No. 7137

Examiner: Ori Nadav

Art Unit: 2811

**RESPONSE TO NOTICE  
OF NON-COMPLIANT  
APPELLANTS' BRIEF  
UNDER 37 CFR §41.37**

Mail Stop Appeal Brief  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Examiner:

In response to the Notification of Non-Compliant Appeal Brief dated November 6, 2009, Appellant hereby resubmits this Brief in support of its appeal from a final decision by the Examiner, mailed July 25, 2008 in the above-captioned case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

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### **1. REAL PARTY IN INTEREST**

All right, title, and interest in the subject invention and application is assigned to Ixys Corporation, having an office at 3540 Bassett Street, Santa Clara, California, 98054. Therefore, Ixys Corporation is the real party in interest.

### **2. RELATED APPEALS AND INTERFERENCES**

No other appeals or interferences are known which will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal.

### **3. STATUS OF CLAIMS**

Currently pending claims 1-3 and 26-30 are the subject of this appeal. No other claims are pending.

Claims 1-3, 26, 28, and 30 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Yano* (U.S. Patent No. 5,138,415) in view of *Gross* (U.S. Patent No. 5,316,964).

Claims 27 and 29 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Yano* (U.S. Patent No. 5,138,415) and *Gross* (U.S. Patent No. 5,316,964), in view of *Collins* (U.S. Patent No. 5,262,754).

Claims 4-25 have been canceled.

### **4. STATUS OF AMENDMENTS**

Claims 1-30 were pending at the time of the Final Office Action dated March 6, 2008. Claims 4-25 were previously withdrawn pursuant to a restriction requirement dated May 4, 2004, and, as such, claims 4-25 were canceled by an amendment after final dated December 29, 2008 in order to place the application in better form for appeal by reducing the issues. As such, claims 1-3 and 26-30 are currently pending and are the subject of this appeal. No other claims are pending. A copy of all the pending claims involved in the present appeal is provided in the Claims Appendix attached hereto.

## **5. SUMMARY OF CLAIMED SUBJECT MATTER**

The present invention relates to a power device; e.g., a diode, a transistor, a thyristor, and the like. Prior to the present invention, 5" wafer fabrication processes typically employed a glass passivation layer on a wafer. However, employing a glass passivation layer on wafers larger than 5", e.g., 6" or 8", tended to bend the wafer. (*Specification*, paragraph [0019]). In substituting the glass passivation layer with a non-glass passivation layer to avoid bending, it was recognized that (a) the reverse blocking voltage of the resulting device was lowered, and (b) the resulting device had an increased leakage current. (*Specification*; paragraphs [0030] and [0031]). Advantageously, the use of a peripheral junction region as claimed at least overcomes these deficiencies. (*Specification*, paragraphs [0032] and [0038]). In other words, the claimed peripheral junction region at least advantageously increases the reverse blocking voltage and decreases the leakage current of a power device.

Independent claim 1 recites a power device (54 in Figure 3, 56 in Figure 4, 60 in Figure 6) (see *Specification* in at least paragraph [0005], line 1; paragraph [0034], line 1; paragraph [0042], line 1; and paragraph [0046], lines 1-2). As shown in Figures 3, 4 and 6, the power device includes a semiconductor substrate (1) of first conductivity having an upper surface (3) and a lower surface (4) (see *Specification* in at least paragraph [0005], lines 1-2; and paragraph [0035], lines 1-2). The power device further includes a first electrode terminal (7) coupled to a first conductive region (5, 7(b), 14) provided proximate the upper surface (3) of the substrate (1), the first electrode terminal (7) being provided over the upper surface (3) of the substrate (1) (see *Specification* in at least paragraph [0039], lines 1-2; and paragraph [0041], line 1). The power device further includes a second electrode terminal (16) coupled to a second conductive region (15) provided proximate the lower surface (4) of the substrate (1), the second electrode terminal (16) being provided below the lower surface (4) of the substrate (1) (see *Specification* in at least paragraph [0041], lines 1-2). The power device further includes an isolation diffusion region (2) of second conductivity provided at a periphery of the substrate (1) and extending from the upper surface (3) to the lower surface (4) of the substrate (1), the isolation diffusion region (2) having a first surface corresponding to the upper surface (3) of the substrate (1) and a second surface corresponding to the lower surface (4) (see *Specification* in at

least paragraph [0005], lines 2-6; and paragraph [0035], lines 1-2). The power device further includes a peripheral junction region (9) of second conductivity formed at least partly within the isolation diffusion region (2) and formed proximate the first surface of the isolation diffusion region (2) (see *Specification* in at least paragraph [0005], lines 6-8; and paragraph [0038]; lines 1-2). The power device further includes a passivation layer (11, 12) provided over the upper surface (3) of the substrate (1), the first surface of the isolation diffusion region (2), and the peripheral junction region (9) (see *Specification* in at least paragraph [0036], lines 1-2). The peripheral junction region (9) is different than the first (5, 7(b), 14) and second (15) conductive regions, and the first (7) and second (16) electrode terminals define a vertical electrical current path therebetween (see Figures 3, 4 and 6).

Claim 2 recites that the peripheral junction region (9) is a P+ region and the isolation diffusion region (2) is a P region. This feature is discussed in the *Specification* in at least paragraph [0038], line 2; and Figures 3, 4 and 6.

Claim 3 recites that the peripheral junction region (9) is provided to compensate the surface depletion of dopants in the isolation diffusion region (2). This feature is discussed in the *Specification* in at least paragraph [0038], lines 4-7.

Claim 26 recites that the passivation layer (11, 12) includes an oxide layer (11) and contacts the upper surface of the substrate (1), the first surface of the isolation diffusion region (2), and the peripheral junction region (9). This feature is discussed in the *Specification* in at least paragraph [0036], lines 1-2; paragraph [0038], lines 1-2; and Figures 3, 4, and 6.

Claim 27 recites that the passivation layer (11, 12) includes a polymid layer (12) over the oxide layer (11). This feature is discussed in the *Specification* in at least paragraph [0036], lines 1-2; and Figures 3, 4, and 6.

Claim 28 recites that the peripheral junction region (9) is provided to compensate the surface depletion of dopants in the isolation diffusion region (2) and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region (2). This feature is discussed in the *Specification* in at least paragraph [0038], lines 2-7.

Claim 29 recites that the passivation layer (11, 12) includes a polyimide layer (12). This feature is discussed in the *Specification* in at least paragraph [0036], lines 1-2; and Figures 3, 4, and 6.

Claim 30 recites that the device (56, 60) is a diode and the first electrode terminal (7) being separated from the isolation diffusion region (2). This feature is discussed in the *Specification* in at least paragraph [0042], lines 2-3; paragraph [0046], lines 2-4; and Figures 4 and 6.

## **6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

Whether claims 1-3, 26, 28, and 30 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over *Yano* (U.S. Patent No. 5,138,415) in combination with *Gross* (U.S. Patent No. 5,316,964).

Whether claims 27 and 29 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over *Yano* and *Gross*, and further in view of *Collins* (U.S. Patent No. 5,262,754).

## **7. ARGUMENT**

No admissions are made by the grouping of claims. Appellant reserves the right to pursue any claims that are not specifically argued in the subsequent prosecution of the present application, and in any continuation application.

### **A. Claims 1-3 and 26-30 were improperly rejected under 35 U.S.C. § 103(a).**

In the Final Office Action dated March 6, 2008, claims 1-3, 26, 28, and 30 were rejected as being unpatentable under 35 U.S.C. § 103(a) over *Yano* in view of *Gross*. Claims 27 and 29 were rejected as being unpatentable under 35 U.S.C. § 103(a) over *Yano* and *Gross*, in view of *Collins* (U.S. Patent No. 5,262,754). Appellant respectfully traverses these rejections for at least the following reasons, which are further set forth below. First, the Examiner failed to properly ascertain the scope and content of the prior art, and also failed to consider the differences between the prior art and the claimed invention. Second, the Examiner has not

articulated any real rationale as to why the cited references should be combined; in fact, the cited references teach against the proposed combination.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *In re Fine*, 5 USPQ2d 1596, 1598, 1599 (Fed. Cir. 1988); MPEP § 2142. *See also In re Piasecki*, 223 USPQ 785, 787, 788 (Fed. Cir. 1984). To establish a *prima facie* case of obviousness, the Examiner must clearly articulate a reason that would have prompted a person of ordinary skill in the relevant field at the time of the invention to modify a reference or combine reference teachings so as to achieve the claimed invention. *KSR Int'l Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (S. Ct. 2007); MPEP §§ 2142. *See also In re Kahn*, 78 USPQ2d 1329, 1335 (Fed. Cir. 2006). A case of obviousness requires ascertaining the scope and contents of the prior art, level of ordinary skill in the art, the differences between the cited references and the claims at issue, and any objective indicia of non-obviousness. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966); *KSR* at 1391. The analysis must consider whether the claimed invention "as a whole" would have been obvious when the invention was unknown and just before it was made. *KSR* at 1391; MPEP § 2142. The ultimate determination of patentability is based on a preponderance of evidence. *In re Oetiker*, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); MPEP § 2142.

For the reasons set forth in detail below, Appellant respectfully submits that a *prima facie* case of obviousness has not been established by a preponderance of evidence for claims 1-3 and 26-30.

1. **The Examiner failed to properly ascertain the scope and content of the prior art, and also failed to consider the differences between the prior art and the claimed invention.**

Independent claim 1, from which claims 2, 3 and 26-30 depend, reads as follows:

*A power device, comprising:*

*a semiconductor substrate of first conductivity having an upper surface and a lower surface;*

*a first electrode terminal coupled to a first conductive region provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;*

*a second electrode terminal coupled to a second conductive region provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;*

*an isolation diffusion region of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface;*

*a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region; and*

*a passivation layer provided over the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region;*

*wherein the peripheral junction region is different than the first and second conductive regions, and*

*wherein the first and second electrode terminals define a vertical electrical current path therebetween.*

[Emphasis provided]

The Examiner failed to properly ascertain the scope and content of the prior art. One having ordinary skill in the art reviewing the full scope and content of the prior art would not be prompted to combine the cited references to achieve the claimed invention.

*Yano*, the primary cited reference, is directed to a photo-semiconductor device. (*Yano*, Abstract). The photo-semiconductor device includes, *inter alia*, a Zener diode (14), a MOSFET (13), and a thyristor (11), all formed in a substrate (16). (*Yano*, col. 5, lines 9-17 and



Fig. 2). A P-type impurity is selectively introduced into the substrate (16) to form a P<sup>+</sup> element isolation region (17) and an anode region (18). (*Yano*, col. 5, lines 20-24). The element isolation region (17) is formed surrounding the Zener diode (14), the MOSFET (13), and the thyristor (11). (*Yano*, col. 5, lines 24-28).

*Gross*, the secondary cited reference, is directed to a method of forming an integrated circuit having diffused resistors located in isolation regions. (*Gross*, Abstract). The integrated circuit includes, *inter alia*, a P-type resistor (23) formed in an N- diffusion region, an NPN transistor formed in a P-type diffusion region adjacent the P-type resistor (23), and a PNP transistor formed in a P-type diffusion region adjacent the P-type resistor. (*Gross*, col. 2, lines 13-44 and Fig. 2). N<sup>+</sup> diffusion regions are formed within the N- diffusion region on both sides of the P-type resistor (23) to increase the isolation between, for example, the P-type resistor (23) and adjacent transistors. (*Gross*, col. 2, lines 38-41).

The Examiner admits that *Yano* does not teach a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region is different than the first and second conductive regions, as required by claim 1. (*Final Office Action*, page 3, fourth paragraph). The Examiner attempts to remedy this deficiency of *Yano* by combining the teachings of *Yano* with those of *Gross*. In particular, the Examiner argues that:

Gross teaches in figure 2 and related text a peripheral junction region of second conductivity N<sup>+</sup> formed at least partly within an N type isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a peripheral junction region of second conductivity at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, in *Yano's* device *in order to increase the electrical isolation capabilities of the device*. The combination is motivated by the teachings of *Gross* who points out the advantages of using a peripheral junction region within the isolation junction region (column 2, lines 38-41). (*Final Office Action* dated March 3, 2008, page 3, fifth paragraph)(emphasis added).

In other words, the Examiner alleges that one skilled in the art at the time of filing the subject application would apply a diffusion region like the N+ diffusion region located between, for example, the P-type resistor (23) and P-type isolated region (18) in *Gross* (see *Gross*, figure 2) to the P+ element isolation region (17) in *Yano* (see *Yano*, figure 2).

Appellant disagrees with the Examiner that the claimed invention as a whole is rendered obvious by the combination of *Yano* and *Gross*. Specifically, the Examiner has not properly ascertained the scope and content of the prior art. The Examiner has also failed to consider the differences between the prior art and the claimed invention, which if properly considered would not reasonably lead to establishing a case of obviousness.

The claimed invention and *Yano* are directed to devices in which vertical electrical currents pass between electrode terminals. In contrast, the device of *Gross* is directed to resistors and other semiconductor structures laid out horizontally with respect to one another. While at first glance this appears to be a mere difference in orientation, closer scrutiny of the technologies illustrates that they are, for all practical purposes, substantially different from one another. For example, in *Gross*, it was desired to increase isolation between multiple adjacently deposited but individually operable elements; i.e., resistors, transistors, etc. In contrast, in the claimed invention, it was desired to modify the operating characteristics (e.g., blocking voltage) of a single device; i.e., a thyristor, diode, power device, etc. Accordingly, one skilled in the art at the time of filing the subject application would have no reason to increase the doping level of the P+ element isolation region (17) even further since the vertical structure of *Yano* does not lend itself to requiring isolation from horizontally displaced elements as does the device of *Gross*.

The combination of *Yano* and *Gross* do not teach the claimed invention. Rather, the cited references teach unnecessarily increasing the doping level of an isolation region in a vertical structure to improve isolation from non-existent horizontally displaced elements. Accordingly, the Examiner has not properly ascertained the scope and content of *Yano* and *Gross*. In fact, the Examiner has ignored the differences between the cited references and the claimed invention. For at least these reasons, Appellant respectfully submits that the claimed invention as a whole is not rendered obvious by the combination of *Yano* and *Gross*.

- 2. The Examiner has not articulated any real rationale as to why the cited references should be combined, and has failed to consider aspects of the cited references that teach away from the proposed combination.**

As stated above, the Examiner alleges that one skilled in the art at the time of filing the subject application would apply the diffusion region in *Gross* (see *Gross*, figure 2) to the P+ element isolation region (17) in *Yano* (see *Yano*, figure 2). The reason one skilled in the art would be motivated to do this, the Examiner argues, is to increase isolation in the device of *Yano* similar to the increased isolation achieved in the device of *Gross*. However, the reason indicated by the Examiner is insufficient to have prompted a person of ordinary skill in the relevant field at the time of the invention to modify *Yano* based on *Gross* to achieve the claimed invention. The differences between the claimed invention and the cited references, as articulated above, teach against combining *Yano* and *Gross*. Specifically, one skilled in the art at the time of filing the subject application would have no reason to increase the doping level of the P+ element isolation region even further since the vertical structure of *Yano* does not lend itself to requiring isolation from horizontally displaced elements as does the device of *Gross*.

The reason for applying the isolative N+ diffusion region in *Gross* does not exist in *Yano*. In accordance with the method of forming an integrated circuit in *Gross*, immediately after the NPN transistor, P-type resistor, and PNP transistor are formed, they are merely separated via an N- diffusion region (17) and P-type region (18). (*Gross*, col. 2, lines 13-32). In other words, an N-type region having a relatively low doping amount along with a P-type region form a (relatively weak) PN junction which isolates the elements (such as the resistor (23) and adjacent transistors) of the integrated circuit from one another. Likely due to the N-type region having a relatively low amount of doping, the method in *Gross* provides for an additional step to "beef up" the relatively low doping level so as to create an N+ diffusion region (*Gross*, col. 2, lines 38-41). The N+ diffusion region thus forms a (relatively strong) PN junction having higher insulation properties than the previously existing PN junction formed via an N- region.

This situation, however, is not evident in the device of *Yano*. Rather, the element isolation region (17) in *Yano's* device is already a relatively heavily doped region, as indicated by

the P+ in figure 2. (*Yano*, col. 5, lines 20-24). Accordingly, since the element isolation region (17) in *Yano* is already relatively heavily doped, one skilled in the art at the time of filing the subject application would not see any need, desire, or advantage in providing another method step to increase the doping level in the element isolation region (17) even more.

Regardless of the differences between the claimed invention and the cited art, the Examiner has failed to provide a rationale to combine *Yano* and *Gross*. Specifically, the differences between the cited references and the claimed invention teach against combining *Yano* and *Gross* for at least the following reasons. First, the *Yano* device has a structure that is entirely different than that of *Gross*. Second, the claimed invention is more than the predictable use of prior art elements according to their established functions.

a. The *Yano* device has a structure that is entirely different than that of *Gross*.

As previously articulated by Appellant, the *Yano* device has a structure that is entirely different than that of *Gross*. (*Appellant Response Dated July 11, 2008*, page 10, second paragraph and page 11, second paragraph).

The claimed invention and device in *Yano* are generally directed to high power devices such as thyristors, diodes, and the like. (*Specification*, paragraph [0003]; *Yano*, col. 5, lines 29-31). Power devices are typically understood to be discrete devices; i.e., after fabrication, power devices are typically employed as discretely encased elements. In contrast, *Gross* describes an integrated circuit; i.e., after fabrication, the circuit described in *Gross* is typically integrated with other elements within the same substrate. Since the circuit described in *Gross* is typically integrated with other elements within the same substrate, there clearly exists a desire to isolate the elements of *Gross*, such as the resistor and transistors, not only from one another but also from other elements that are integrated within the same substrate. However, such isolation issues do not exist in discrete devices since no other elements are provided post-fabrication within the same substrate. Accordingly, such isolation issues do not exist in either the claimed invention nor the device of *Yano*.

In particular, since the device of *Yano* is likely a discrete device, there are no post-fabrication elements located in *Yano's* substrate (16) other than the Zener diode (14), MOSFET (13), and thyristor (11). In other words, with reference to figure 2 of *Yano*, there simply are no post-fabrication elements located in the substrate (16) to the left of the left-most label (17) nor to the right of the right-most label (17). Accordingly, one skilled in the art at the time of filing the subject application would have no reason to increase the doping level of the P+ element isolation region (17) even further since there are no elements located in the substrate (16) outside of the Zener diode (14), MOSFET (13), and thyristor (11) which the Zener diode (14), MOSFET (13), and thyristor (11) need to be isolated from.

The Examiner's response to this argument is that "a power device is an integrated circuit." (*Advisory Action Dated July 25, 2008*, page 2, second last paragraph). However, Appellant respectfully submits that a power device is not necessarily "an integrated circuit," but rather may *include* an integrated circuit. Moreover, a power device as envisioned by the claimed invention and *Yano* is a discrete structure, whereas the integrated circuit in *Gross* is not a discrete structure.

b. The claimed invention is more than the predictable use of prior art elements according to their established functions.

As previously articulated by Appellant, the claimed invention is more than the predictable use of prior art elements according to their established functions. (*Appellant Response Dated July 11, 2008*, page 11, last paragraph). The heavily doped N+ diffusion regions of *Gross* are used to increase isolation. (*Gross*, col. 2, lines 38 to 41) Consequently, assuming – although Appellant disagrees with – the combination of *Yano* and *Gross* as suggested by the Examiner, by incorporating such diffusion regions into the isolation diffusion region (17) of *Yano*, one skilled in the art at the time of filing the subject application would merely predict that the thyristor (11) and capacitor (C1) in *Yano's* device would be better isolated from adjacent semiconductor elements, if any, located outside of the isolation region (17) (see *Yano*, figure 2).

One would not predict that the operating characteristics of the thyristor (11) itself would be modified.

Indeed, the inventor of the present application is believed to be the first individual to publicly recognize the effect on operating characteristics of a thyristor and the like by incorporating peripheral junction regions as illustrated in, for example, figure 3. This is evidenced by at least the fact that *Yano* used an oxide film (28) that likely caused surface depletions in the isolation diffusion region (17) resulting in decreased reverse blocking voltages. However, *Yano* failed to point out such problems and possible remedying effects of incorporating peripheral junction regions. In contrast, such problems and remedying effects of a peripheral junction region are exactly what the inventor of the claimed invention recognized in his endeavor to expand wafer size while avoiding bending problems. (*Specification*, paragraphs [0029]-[0031] and [0038]).

The Examiner's response to this argument is:

Certainly, Gross uses his isolation structure to provide isolation to elements in the disclosed structure and not to provide isolation to elements which are not present in the disclosed structure. When using the isolation structure of Gross in a different structure, the isolation structure will isolate the elements of said different structure. (*Advisory Action*, page 3, second last paragraph).

According to the U.S. Supreme Court, when determining whether one skilled in the art would have combined the teachings of multiple prior art, "a court *must* ask whether the improvement is *more than* the predictable use of prior art elements according to their established functions." *KSR* at 1396. (emphasis added). As recognized by the Examiner, the established function of the N+ type diffusion region at issue in *Gross* is "to increase isolation." (*Gross*, col. 2, lines 38-41). However, the claimed peripheral junction region does *more than* this; the claimed peripheral junction region at least functions to increase the reverse blocking voltage of the device. (*Specification*, paragraph [0038]). Accordingly, the claimed invention is more than the predictable use of prior art elements according to their established functions.

For at least these reasons, Appellant respectfully submits that the Examiner has not articulated any real rationale as to why the cited references should be combined; in fact, the cited references teach against the proposed combination.

**3. Regarding claim 28, *Yano* does not teach a peripheral junction region.**

Claim 28 reads as follows:

*The device of claim 1, wherein the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region.*

As previously articulated by Appellant (*Appellant Response Dated July 11, 2008*, page 12, last paragraph to page 13, third paragraph), the Examiner asserts that *Yano* teaches, in figure 2, "a power device, comprising: ... wherein the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region." (*Final Office Action dated Mar. 6, 2008*, page 3, third paragraph). However, the Examiner also asserts, and Appellant agrees, that "*Yano* does not teach a peripheral junction region." (*Final Office Action dated Mar. 6, 2008*, page 3, fourth paragraph). Since *Yano* does not teach a peripheral junction region, it logically follows that *Yano* cannot teach a more specific peripheral junction region, i.e., a peripheral junction region "that is provided to compensate the surface depletion of the isolation diffusion region."

Moreover, Appellant respectfully submits that *Gross* fails to remedy these deficiencies of *Yano*. The heavily doped N-type diffusion region of *Gross* merely functions to increase isolation. The heavily doped N-type diffusion region does not appear to compensate for a surface depletion of dopants. The combination of *Yano* and *Gross* fails to teach a peripheral junction region provided to compensate the surface depletion of dopants in the isolation diffusion region since there is no teaching or suggestion that the photo-semiconductor device in *Yano* experiences a surface depletion of dopants in the isolation diffusion region (17). Indeed, it is not likely that the devices in *Yano* and *Gross* experienced a significant surface depletion of dopants

since such surface depletion was only recognized by the inventor of the present application as a result of a long diffusion step used to diffuse aluminum into the substrate. (*Specification*, paragraph [0031]). Neither *Yano* nor *Gross* disclose such a long diffusion step much less the resulting surface depletion of dopants. Appellant was unable to locate a response to these arguments in the *Advisory Action*.

For at least these reasons, Appellant respectfully submits that claim 28 is not rendered obvious by *Yano* and *Gross* either alone or in combination with one another. Accordingly, Appellant respectfully submits that claim 28 is allowable for both this reason and those reasons articulated above with respect to independent claim 1.

**4. Regarding claim 30, *Yano* and *Gross* do not teach that the device is a diode.**

Claim 30 reads as follows:

*The device of claim 1, wherein the device is a diode and the first electrode terminal being separated from the isolation diffusion region.*

As previously articulated by Appellant (*Appellant Response Dated July 11, 2008*, page 13, second last paragraph to page 14, second paragraph), the Examiner asserts that the prior art's device includes the device being a diode (*Final Office Action Dated Mar. 6, 2008*, page 4, third paragraph). However, Appellant respectfully submits that neither *Yano* nor *Gross* either alone or in combination teach that the device is a diode.

The device as claimed requires a semiconductor substrate, a first electrode terminal, a second electrode terminal, an isolation diffusion region, etc. (see claim 1). It is the combination of these elements which form the device, and consequently, it is the combination of these elements which form a diode in accordance with claim 30. In *Yano*, there is no similar combination of elements which forms a diode. Rather, the elements of *Yano* which allegedly correspond to the claimed device elements form a thyristor (11). The only diode disclosed in the relevant teachings of *Yano* is the Zener diode (14) illustrated in figure 2. This Zener diode (14) fails to constitute the aforementioned combination since it only includes a P-well region (22), N+



impurity region (27), and electrode (34) (and thus does not constitute the claimed semiconductor substrate, second electrode terminal coupled to a second conductive region provided ... below the lower surface of the substrate, an isolation diffusion region, and a peripheral junction region). *Gross* fails to remedy the deficiencies of *Yano*.

The Examiner's response to these arguments is as follows:

Independent claim 1 recites "a power device, comprising". Dependent claim 30, which must further limit independent claim 1, recites "the device is a diode. " It is understood that a diode must be present in the claimed device. A PN junction is a diode. Therefore, although prior art does not explicitly state the term "diode, " the PN junction present in prior art's device is the claimed diode. (*Advisory Action*, page 4, first paragraph).

Appellant respectfully submits that claim 30 does not limit claim 1 to "include" a diode; in other words, claim 30 does not limit claim 1 such that a diode is "present" in the claimed power device. Rather, claim 30 limits claim 1 such that the power device itself actually is a diode. In other words, claim 30 requires not simply a "power device" to comprise numerous elements; rather, claim 30 requires a specific type of power device (i.e., a diode) to comprise numerous elements. As explained above, Appellant respectfully submits that *Yano* fails to disclose a diode comprising the combination of elements as required by the invention defined by the combination of claims 1 and 30.

For at least these reasons, Appellant respectfully submits that pending dependent claim 30 is not rendered obvious by *Yano* and *Gross* either alone or in combination with one another. Accordingly, Appellant respectfully submits that claim 30 is allowable for both this reason and those reasons articulated above with respect to independent claim 1.

**5. Claims 27 and 29 are dependent on an allowable base claim.**

Claims 27 and 29 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Yano* and *Gross* in view of *Collins*.

Claim 27 is dependent on claim 26 which is dependent on claim 1, and claim 29 is dependent on claim 1. The rejection of claims 27 and 29 is premised on the assertion that *Yano*

and *Gross* disclose the features recited in claim 1, and *Collins* discloses the remaining features of claims 27 and 29.

As discussed above, however, *Yano* and *Gross* does not disclose or suggest all features recited in claim 1. As best understood, *Collins* does not provide any teaching or suggestion that would remedy this deficiency. Specifically, *Collins* discloses a sheet formed of electrically insulating material such as polymers. (*Collins*, col. 2, lines 50-52). Therefore, the rejection is based on a flawed premise and cannot be maintained.

For at least these reasons, Appellant respectfully submits that pending dependent claims 27 and 29 are not rendered obvious by *Yano*, *Gross* and *Collins* either alone or in combination with one another. Accordingly, Appellant respectfully submits that claims 27 and 29 are allowable for both this reason and those reasons articulated above with respect to independent claim 1.

## **8. CONCLUSION**

In view of the foregoing arguments, Appellant respectfully submits that the Examiner has failed to show, by a preponderance of evidence, a *prima facie* case of obviousness.

The inventor of the subject application recognized at least problems, such as low reverse blocking voltages and high leakage currents, due to surface depletions of aluminum and a relatively high fixed oxide charge when attempting to expand the size of wafers via the use of a non-glass passivation layer. The claimed invention, including the claimed peripheral junction region, at least advantageously remedies these problems. These problems, much less the solutions as claimed in the subject application, were not recognized or addressed in any of the relied upon references.

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For at least these reasons, Appellant respectfully submits that claims 1-3 and 26-30 are not rendered obvious by the cited references (*Yano*, *Gross* and *Collins*) either alone or in combination with one another. Accordingly, Appellant requests that the obviousness rejections of record be reversed.

Respectfully submitted,

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## **9. CLAIMS APPENDIX**

1. (Previously Presented) A power device, comprising:

a semiconductor substrate of first conductivity having an upper surface and a lower surface;

a first electrode terminal coupled to a first conductive region provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

a second electrode terminal coupled to a second conductive region provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

an isolation diffusion region of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface;

a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region; and

a passivation layer provided over the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region;

wherein the peripheral junction region is different than the first and second conductive regions, and

wherein the first and second electrode terminals define a vertical electrical current path therebetween.

2. (Original) The device of claim 1, wherein the peripheral junction region is a P+ region and the isolation diffusion region is a P region.

3. (Previously Presented) The device of claim 1, wherein the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region.

4-25. (Canceled)

26. (Previously Presented) The device of claim 1, wherein the passivation layer includes an oxide layer and contacts the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region.

27. (Previously Presented) The device of claim 26, wherein the passivation layer includes a polyimide layer over the oxide layer.

28. (Previously Presented ) The device of claim 1, wherein the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region.

29. (Previously Presented ) The device of claim 1, wherein the passivation layer includes a polyimide layer.

30. (Previously Presented) The device of claim 1, wherein the device is a diode and the first electrode terminal being separated from the isolation diffusion region.

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**10. EVIDENCE APPENDIX**

None.

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**11. RELATED PROCEEDINGS APPENDIX**

None.